FIG. 1

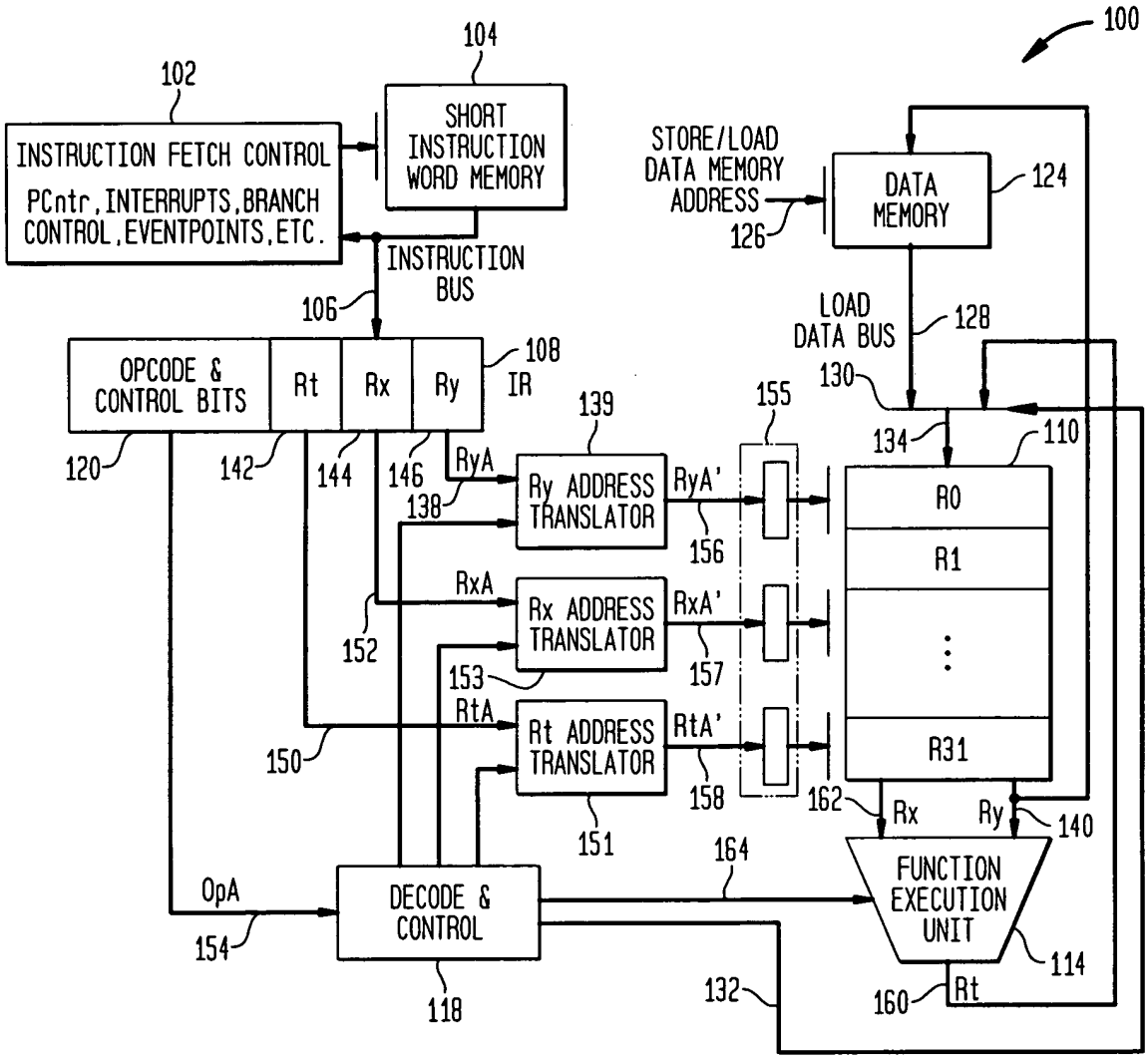


FIG. 2A

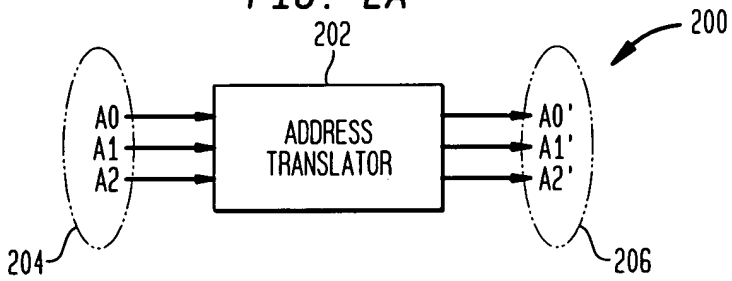


FIG. 2B

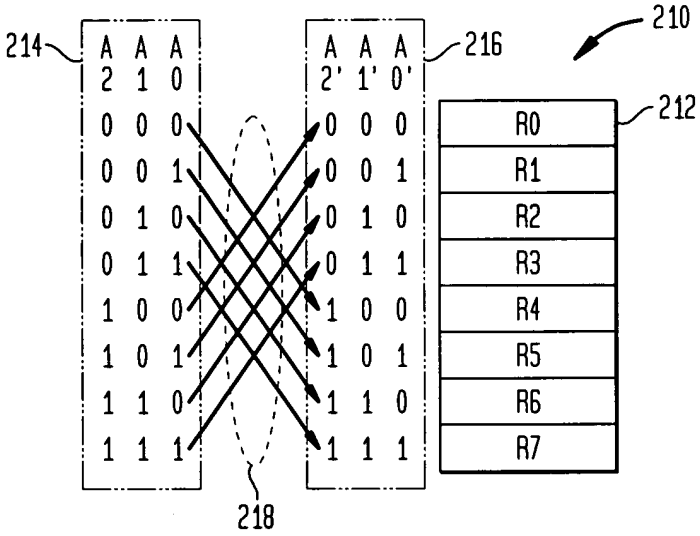


FIG. 2C

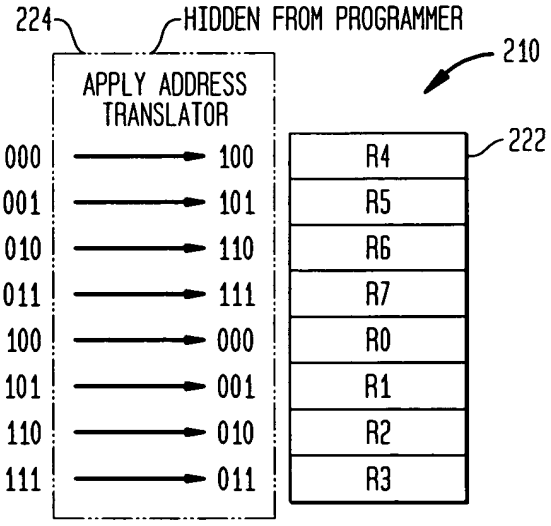


FIG. 2D

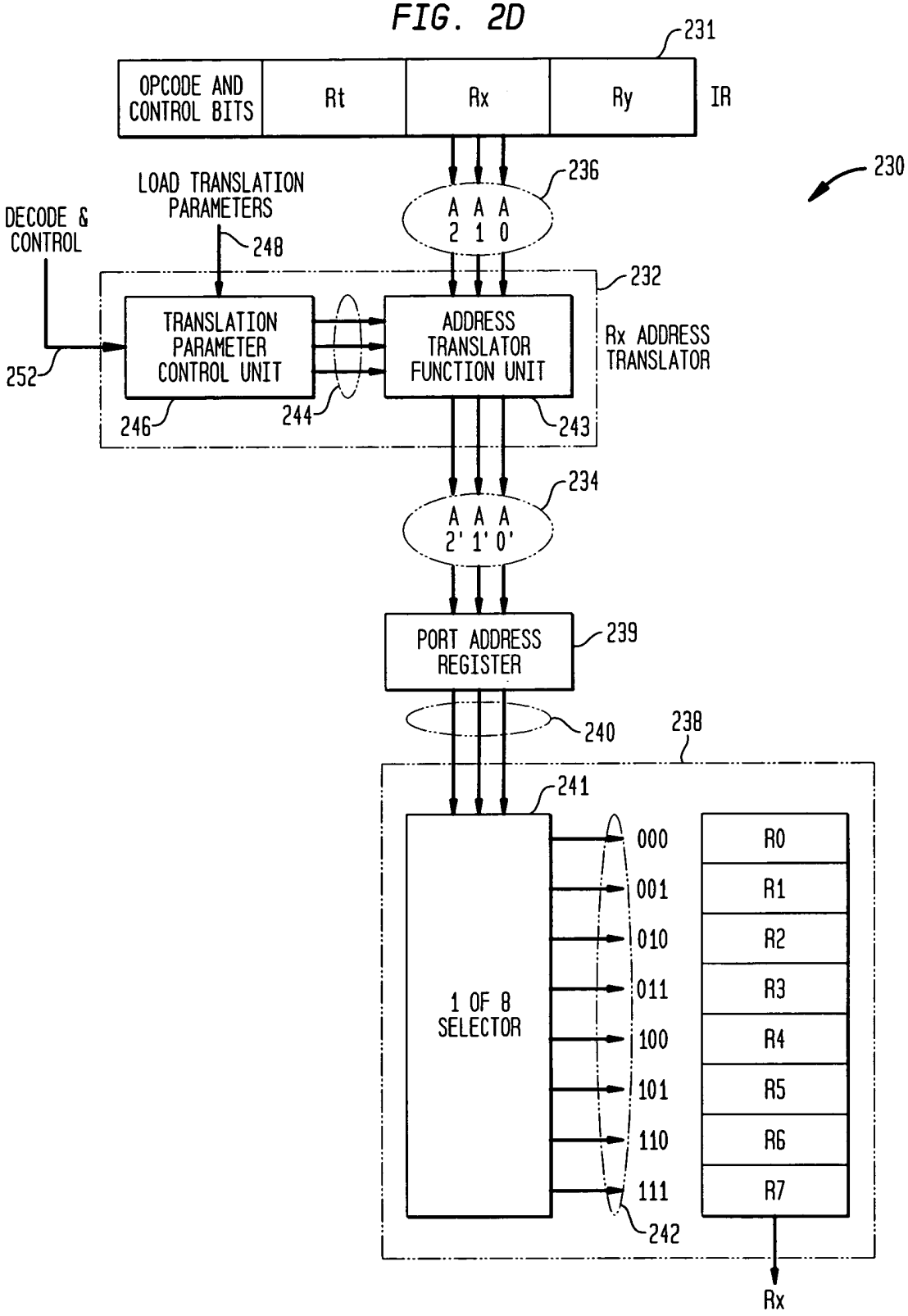

231
OPCODE AND CONTROL BITS
Rt
Rx
Ry
IR
230
236
A A A
2 1 0
LOAD TRANSLATION PARAMETERS
248
DECODE & CONTROL
232
TRANSLATION PARAMETER CONTROL UNIT
ADDRESS TRANSLATOR FUNCTION UNIT
Rx ADDRESS TRANSLATOR
252
246
244
243
234
A A A
2' 1' 0'
PORT ADDRESS REGISTER
239
240
238
241
1 OF 8 SELECTOR
000
001
010
011
100
101
110
111
R0
R1
R2
R3
R4
R5
R6
R7
242
Rx

FIG. 3

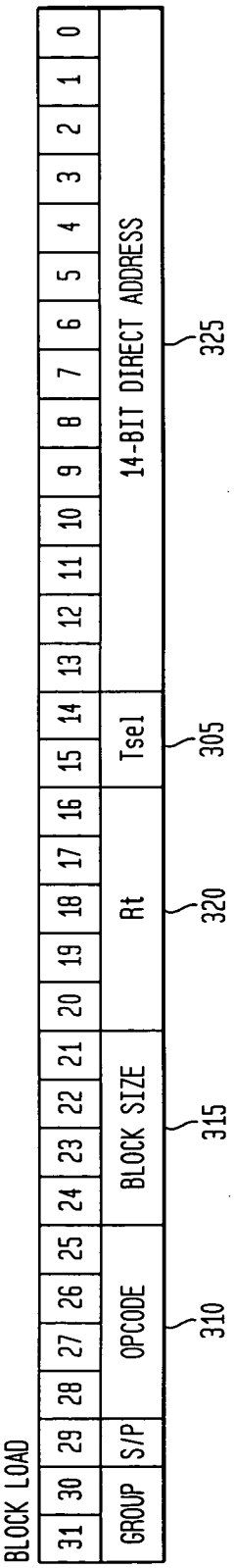

300
BLOCK LOAD
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
GROUP
S/P
OPCODE
BLOCK SIZE
Rt
Tsel
14-BIT DIRECT ADDRESS
310
315
320
305
325

FIG. 4

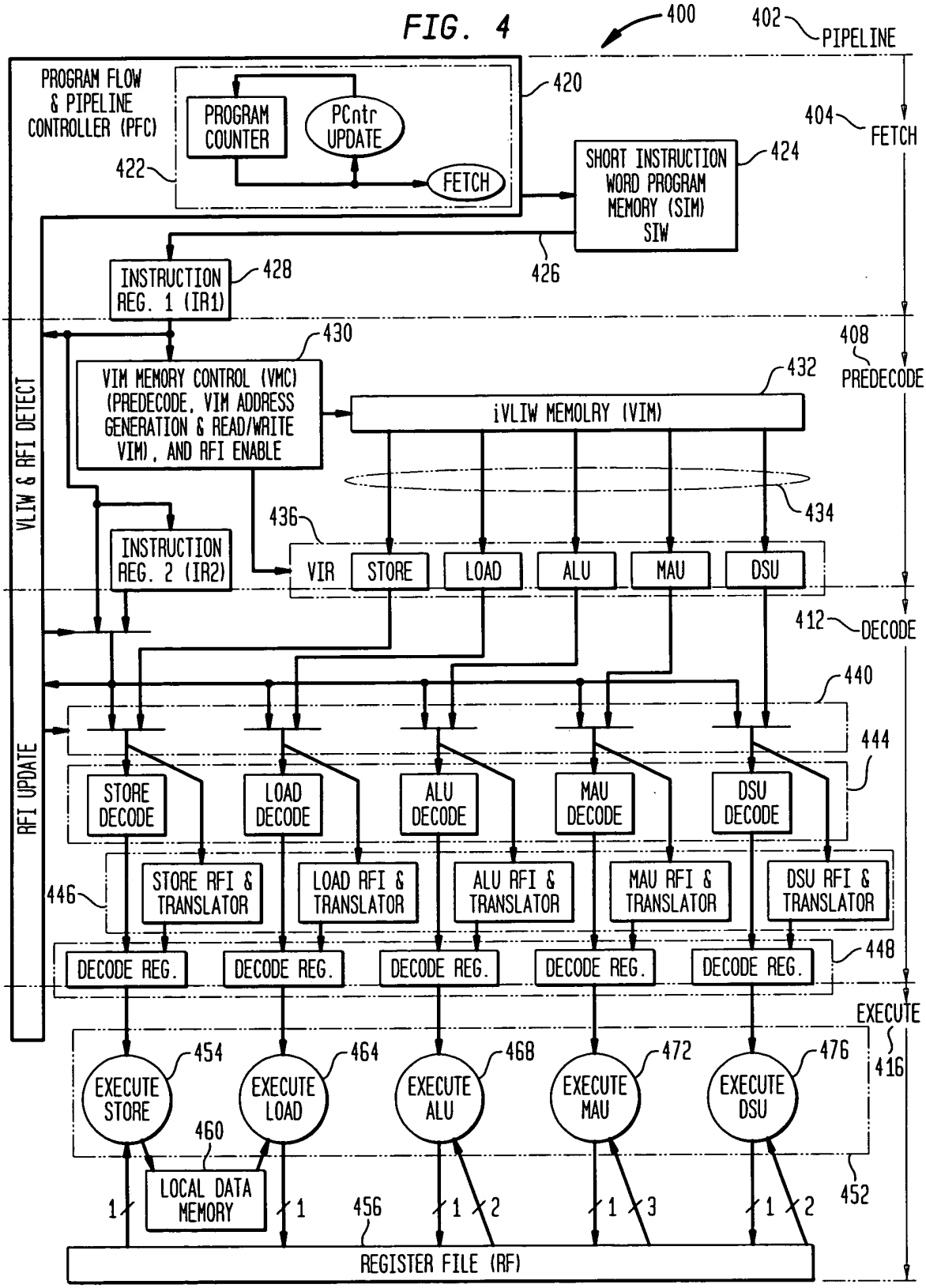

400
402
PIPELINE
PROGRAM FLOW & PIPELINE CONTROLLER (PFC)
420
PROGRAM COUNTER
PCntr UPDATE
FETCH
422
404
FETCH
SHORT INSTRUCTION WORD PROGRAM MEMORY (SIM) SIW
424
426
INSTRUCTION REG. 1 (IR1)
428
VLIW & RFI DETECT
430
VIM MEMORY CONTROL (VMC) (PREDECODE, VIM ADDRESS GENERATION & READ/WRITE VIM), AND RFI ENABLE
408
PREDECODE
432
iVLIW MEMOLRY (VIM)
434
436
INSTRUCTION REG. 2 (IR2)
VIR
STORE
LOAD
ALU
MAU
DSU
412
DECODE
440
444
STORE DECODE
LOAD DECODE
ALU DECODE
MAU DECODE
DSU DECODE
RFI UPDATE
446
STORE RFI & TRANSLATOR
LOAD RFI & TRANSLATOR
ALU RFI & TRANSLATOR
MAU RFI & TRANSLATOR
DSU RFI & TRANSLATOR
DECODE REG.
DECODE REG.
DECODE REG.
DECODE REG.
DECODE REG.
448
EXECUTE
416
454
464
468
472
476
EXECUTE STORE
EXECUTE LOAD
EXECUTE ALU
EXECUTE MAU
EXECUTE DSU
460
LOCAL DATA MEMORY
452
1
1
456
1
2
1
3
1
2
REGISTER FILE (RF)

FIG. 5

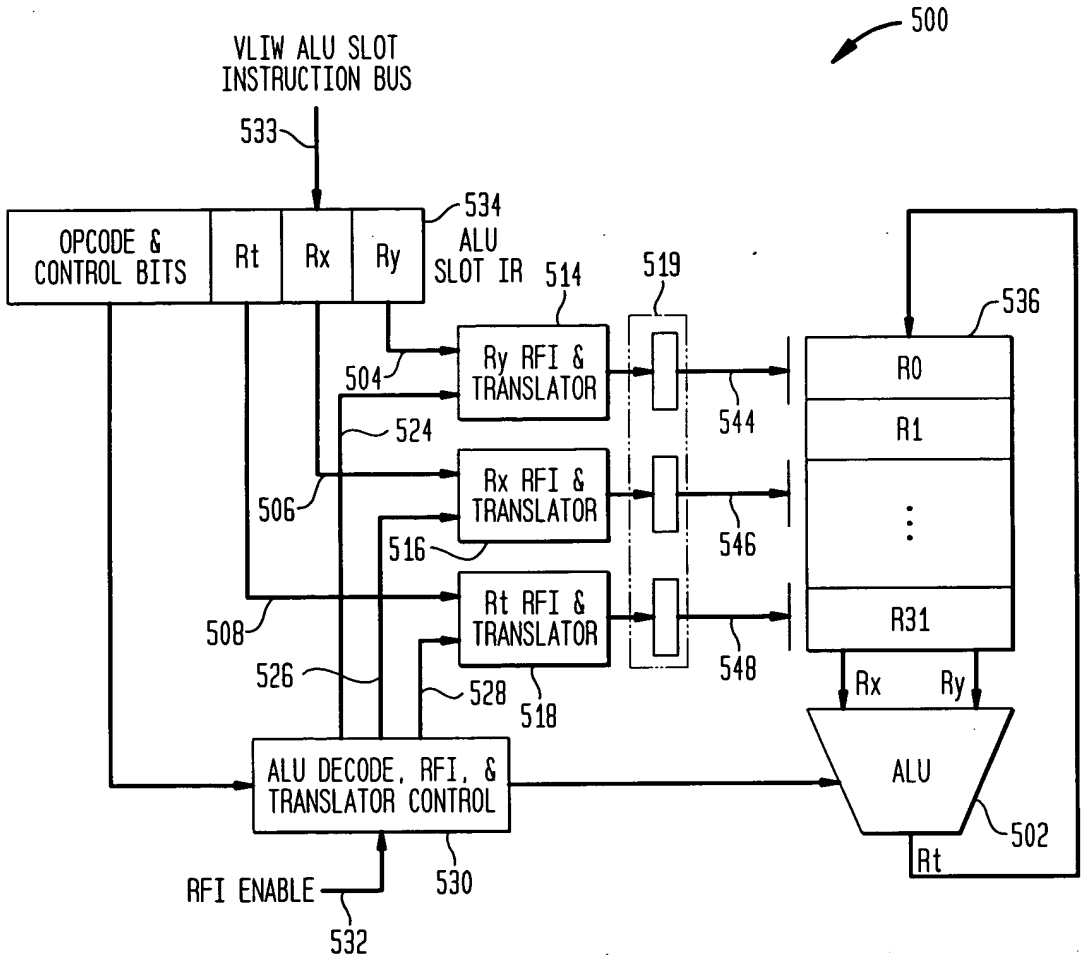

500
VLIW ALU SLOT
INSTRUCTION BUS
533
OPCODE &
CONTROL BITS
Rt
Rx
Ry
534
ALU
SLOT IR
514
519
536
504
Ry RFI &
TRANSLATOR
524
506
Rx RFI &
TRANSLATOR
516
508
Rt RFI &
TRANSLATOR
526
528
518
544
546
548
R0
R1
R31
Rx
Ry
ALU
502
Rt
ALU DECODE, RFI, &
TRANSLATOR CONTROL
530
RFI ENABLE
532

FIG. 6

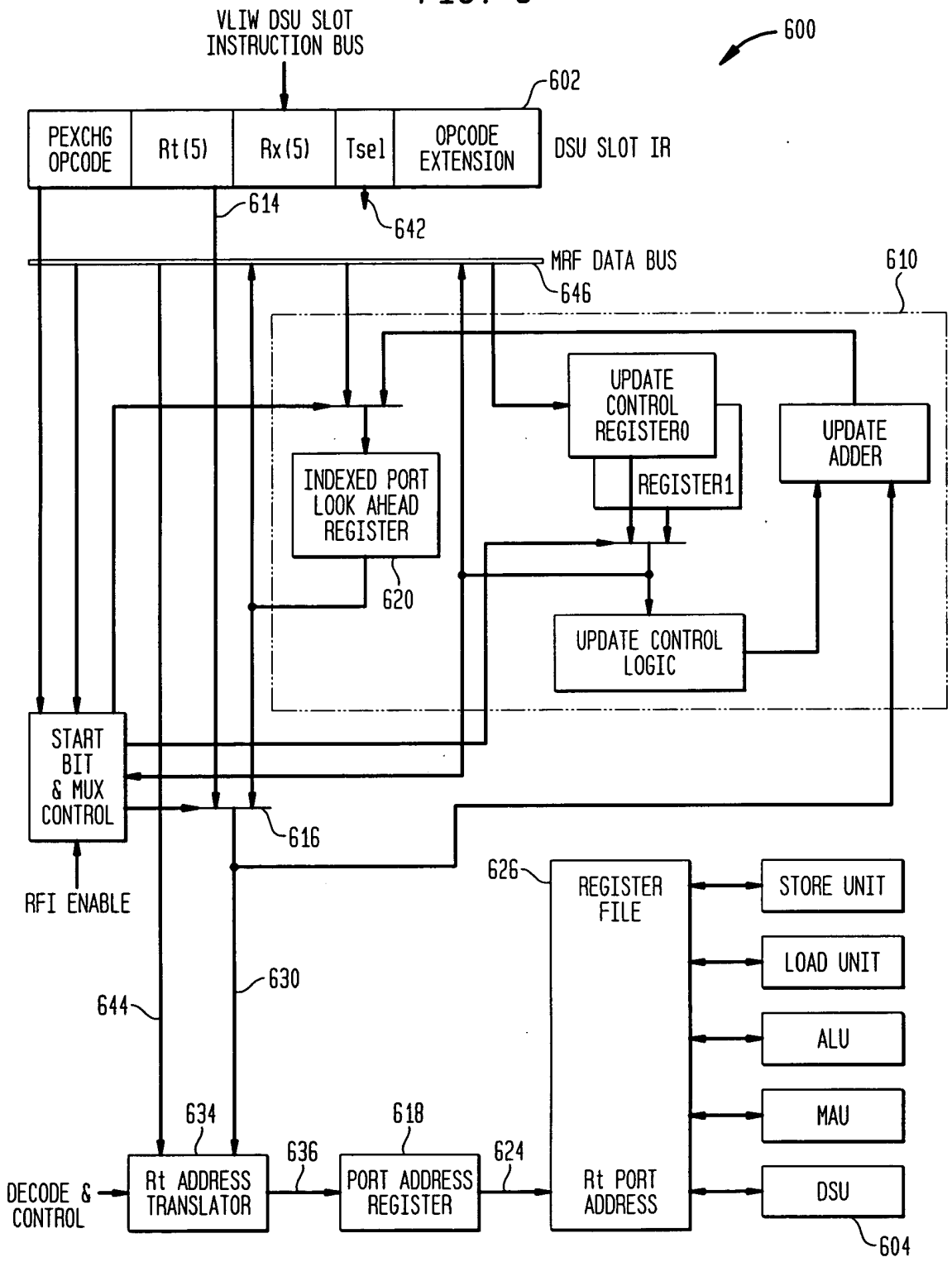

VLIW DSU SLOT INSTRUCTION BUS
600
602
PEXCHG OPCODE
Rt(5)
Rx(5)
Tsel
OPCODE EXTENSION
DSU SLOT IR
614
642
MRF DATA BUS
646
610
UPDATE CONTROL REGISTER0
REGISTER1
UPDATE ADDER
INDEXED PORT LOOK AHEAD REGISTER
620
UPDATE CONTROL LOGIC
START BIT & MUX CONTROL
616
RFI ENABLE
626
REGISTER FILE
STORE UNIT
LOAD UNIT
ALU
MAU
DSU
630
644
634
618
636
624
DECODE & CONTROL
Rt ADDRESS TRANSLATOR
PORT ADDRESS REGISTER
Rt PORT ADDRESS
604

FIG. 7A

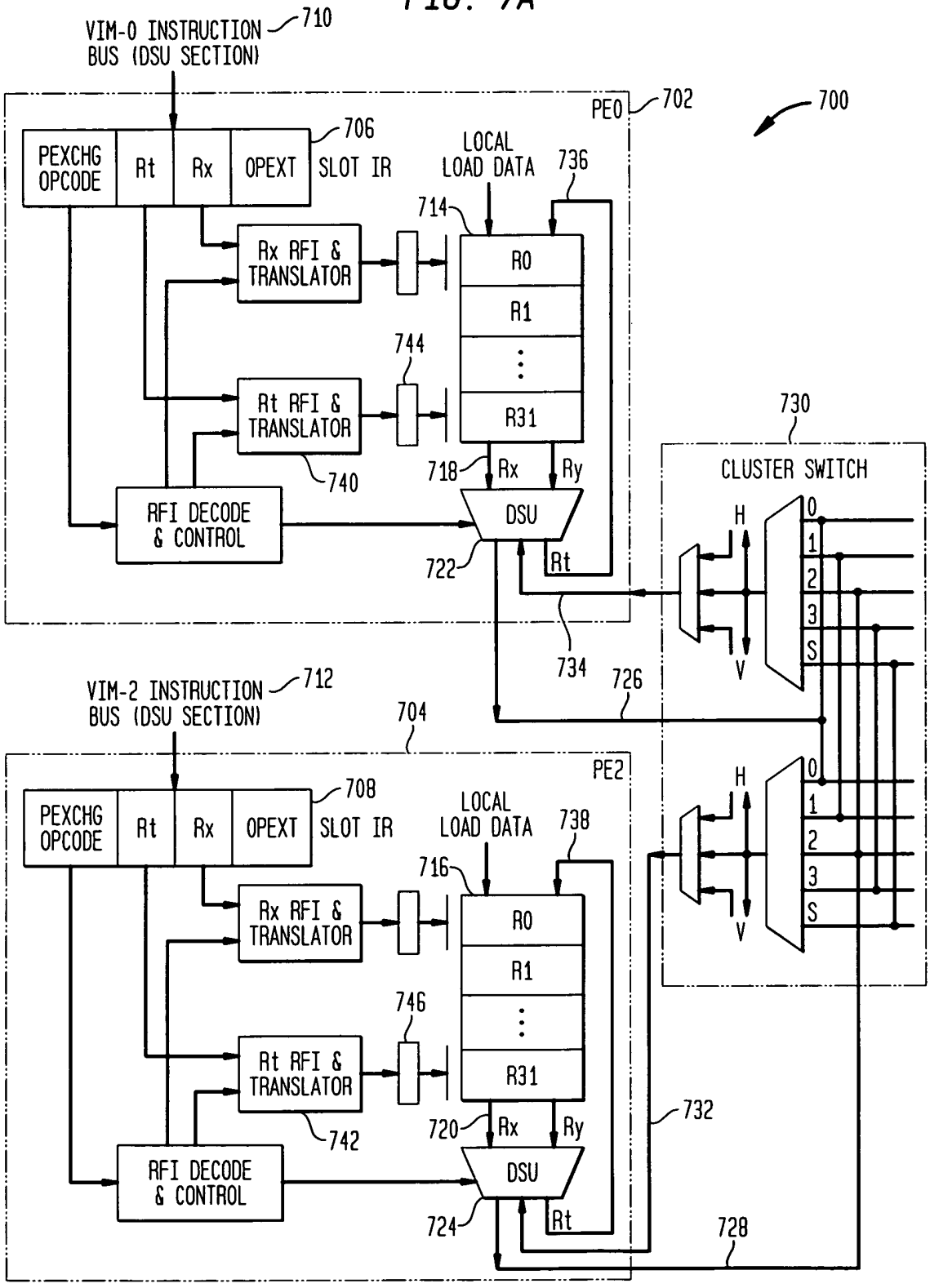

VIM-0 INSTRUCTION BUS (DSU SECTION)
710
PE0
702
700
PEXCHG OPCODE
Rt
Rx
OPEXT
706
SLOT IR
LOCAL LOAD DATA
736
714
Rx RFI & TRANSLATOR
R0
R1
R31
744
Rt RFI & TRANSLATOR
740
730
CLUSTER SWITCH
718
Rx
Ry
RFI DECODE & CONTROL
DSU
722
Rt
H
V
0
1
2
3
S
734
726
VIM-2 INSTRUCTION BUS (DSU SECTION)
712
704
PE2
708
738
716
746
742
720
732
724
728

FIG. 7B

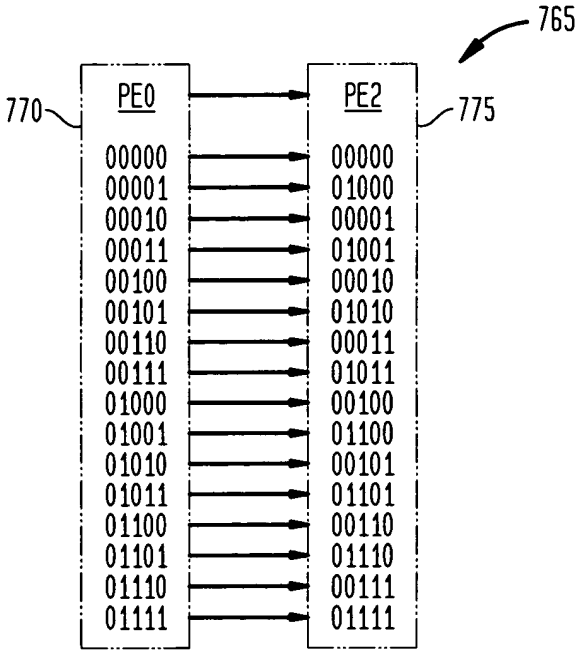

765
770
PE0
PE2
775
00000
00001
00010
00011
00100
00101
00110
00111
01000
01001
01010
01011
01100
01101
01110
01111
00000
01000
00001
01001
00010
01010
00011
01011
00100
01100
00101
01101
00110
01110
00111
01111

FIG. 8A

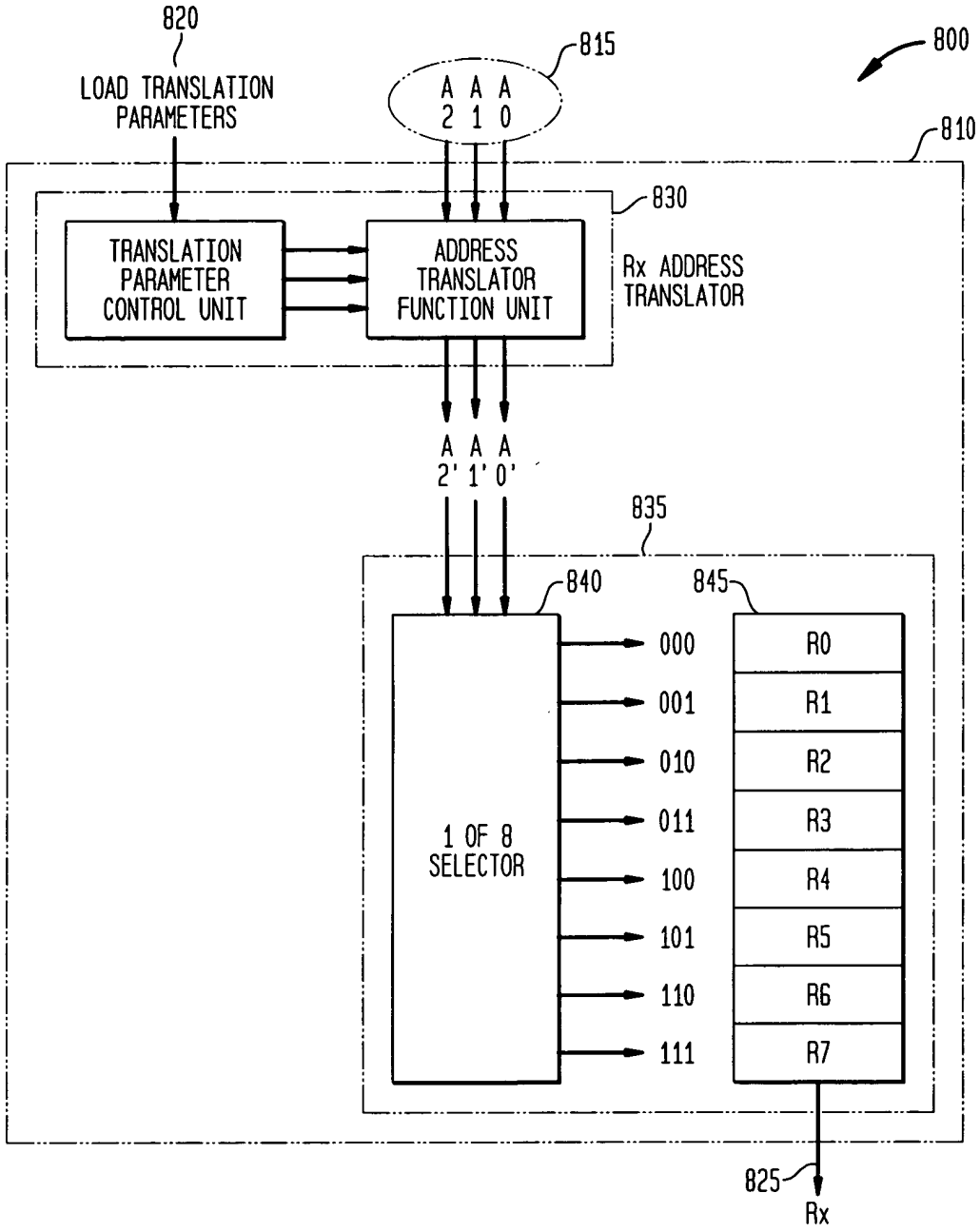

820
LOAD TRANSLATION PARAMETERS
815
A A A
2 1 0
800
810
830
TRANSLATION PARAMETER CONTROL UNIT
ADDRESS TRANSLATOR FUNCTION UNIT
Rx ADDRESS TRANSLATOR
A A A
2' 1' 0'
835
840
845
1 OF 8 SELECTOR
000
001
010
011
100
101
110
111
R0
R1
R2
R3
R4
R5
R6
R7
825
Rx

FIG. 8B

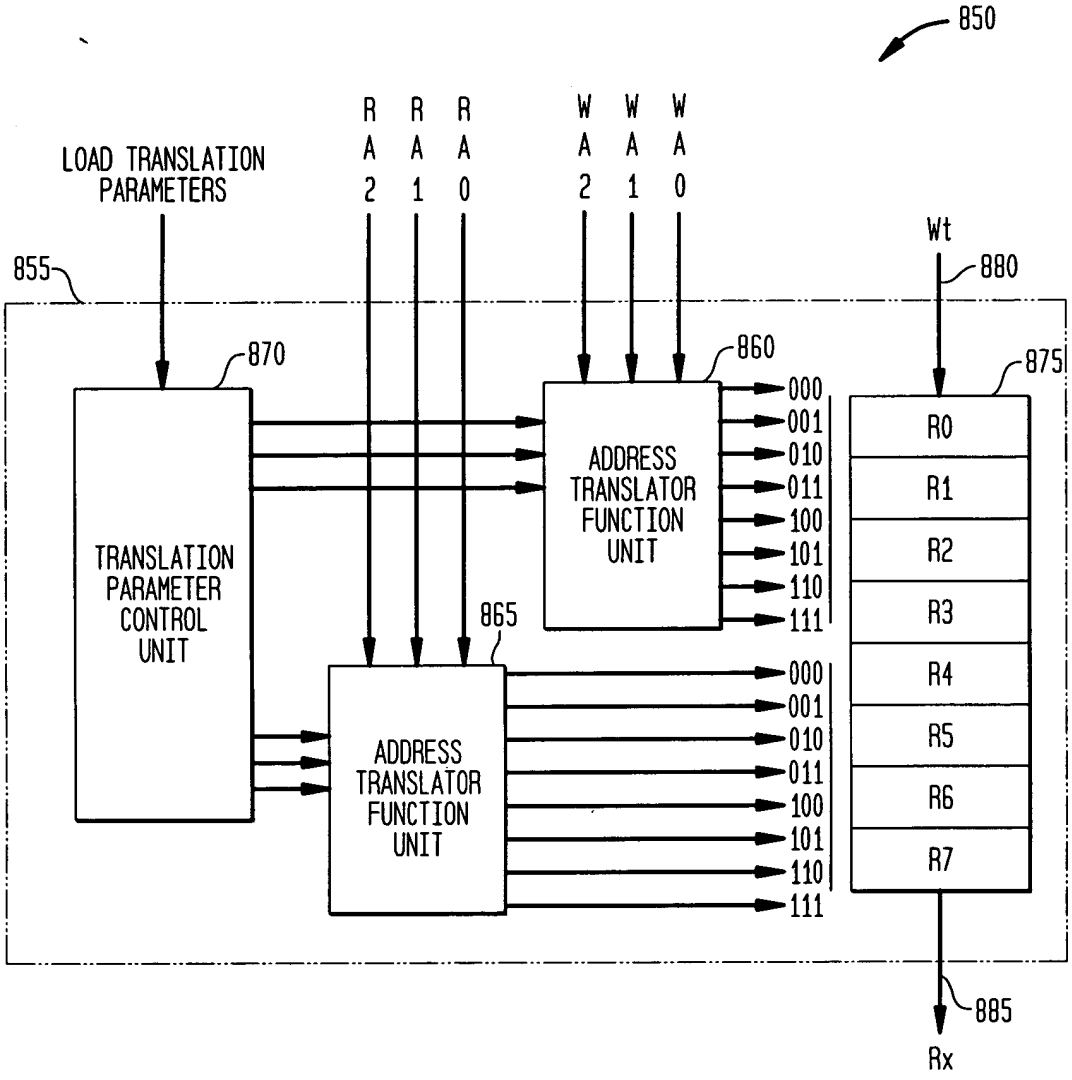
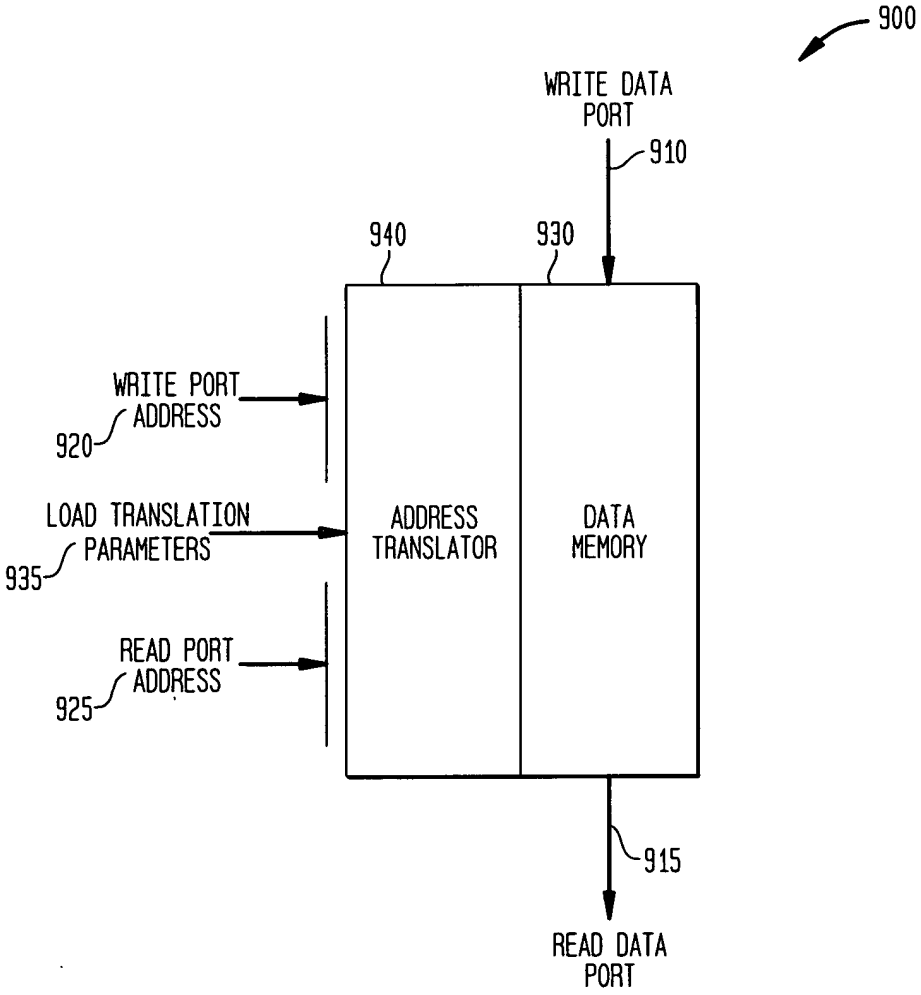

850
LOAD TRANSLATION PARAMETERS
RA2
RA1
RA0
WA2
WA1
WA0
Wt
855
880
870
860
875
TRANSLATION PARAMETER CONTROL UNIT
ADDRESS TRANSLATOR FUNCTION UNIT
000
001
010
011
100
101
110
111
R0
R1
R2
R3
R4
R5
R6
R7
865
ADDRESS TRANSLATOR FUNCTION UNIT
000
001
010
011
100
101
110
111
885
Rx

FIG. 9


900
WRITE DATA PORT
910
940
930
WRITE PORT ADDRESS
920
LOAD TRANSLATION PARAMETERS
935
READ PORT ADDRESS
925
ADDRESS TRANSLATOR
DATA MEMORY
915
READ DATA PORT

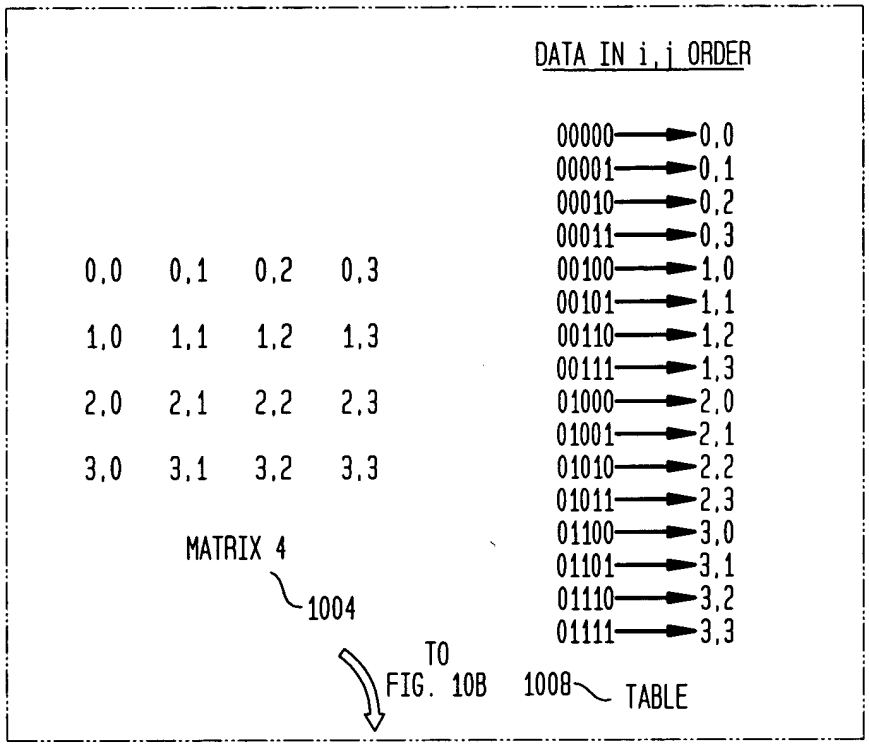


FIG. 10A

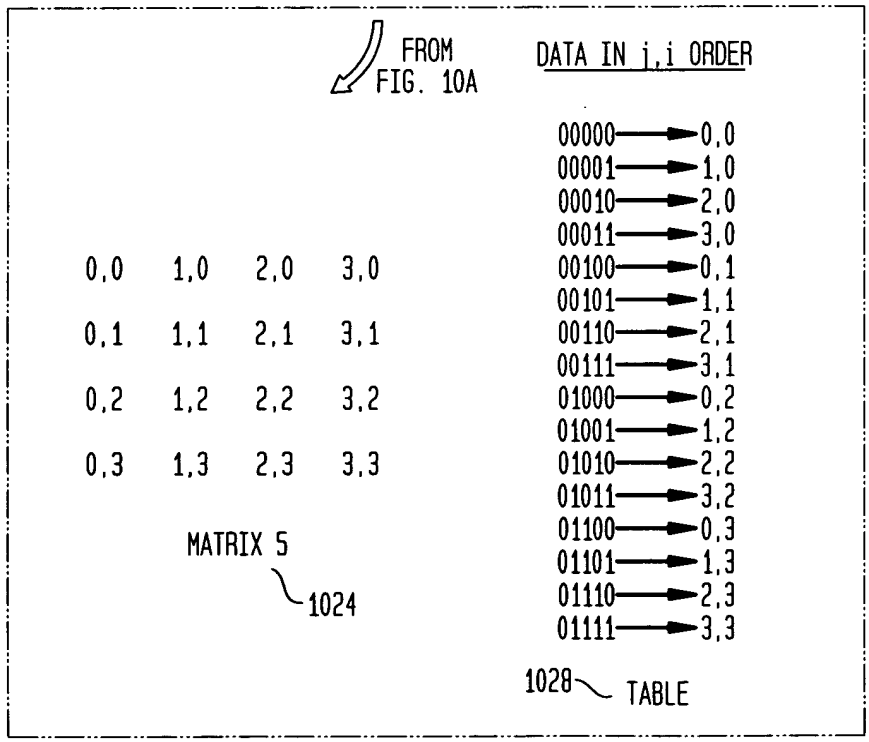


FIG. 10B